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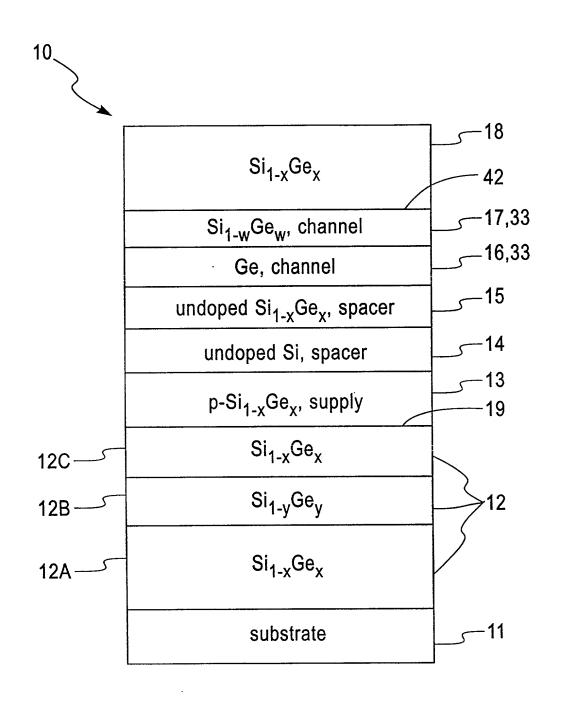


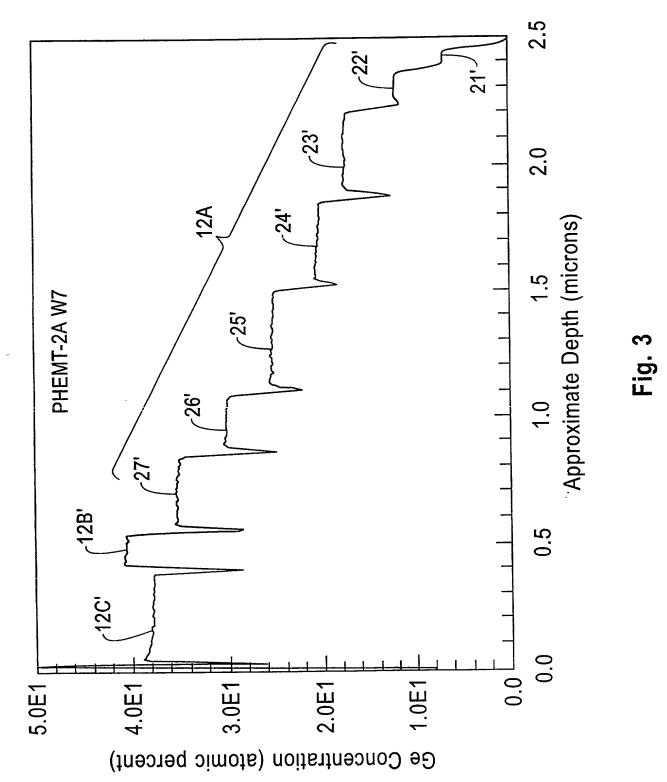
Fig. 1

- Cap si and SiGe Device Layers Strain Relief Layers -Silicon Substrate Thick Buffer 450 nm -11,31 ~33 12C \_\_ 25' — 12B ¬ ∑27' ¬ 23' – 22' – 22' – 21' – **- 26** -24' 12A<

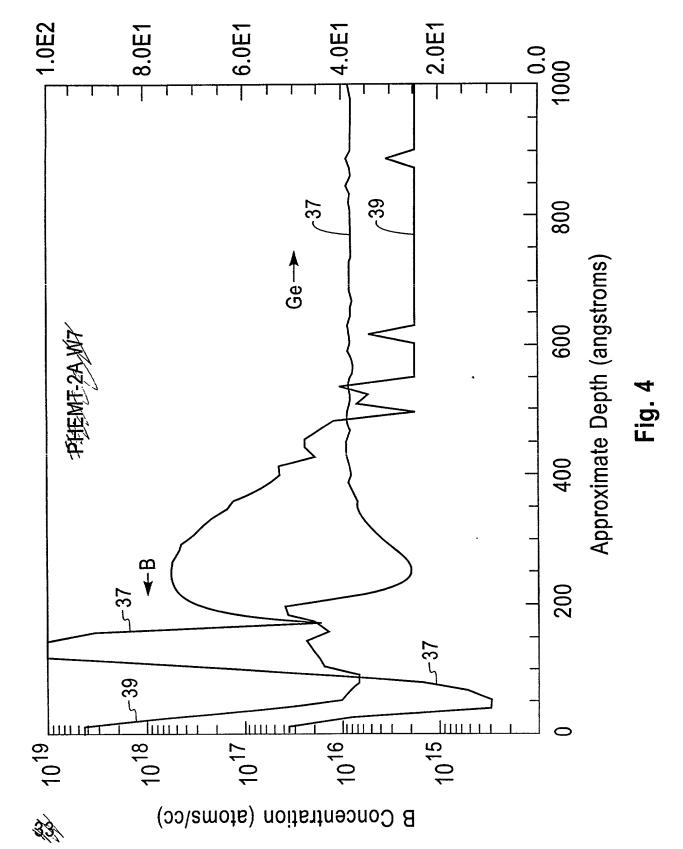
XTEM of PHEMT 2.3 Structure

Fig. 2

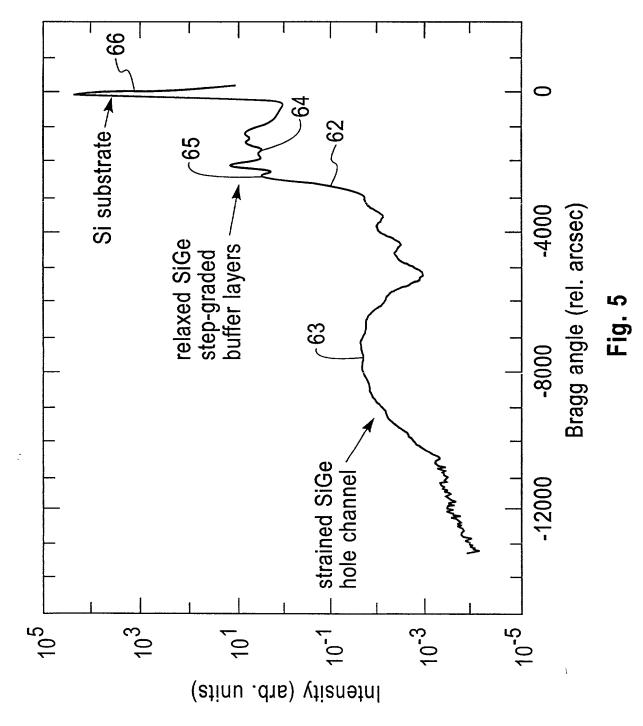
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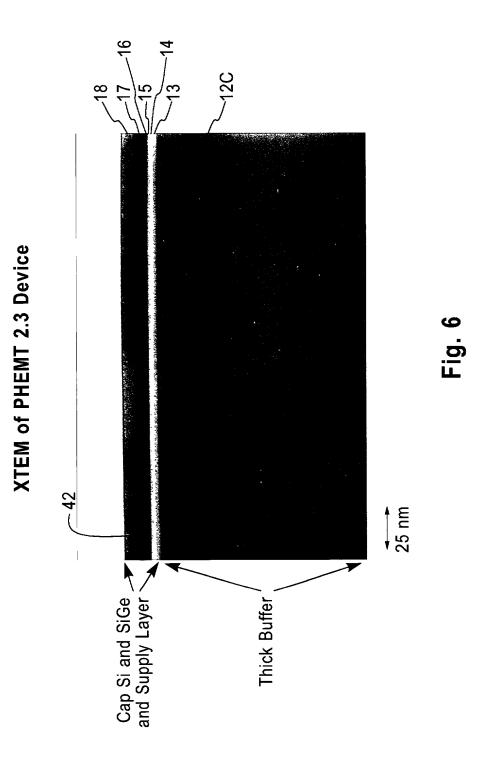


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Stacking fault densities  $\sim 10^6$  -  $10^8/\text{cm}^2$ 



Fia. 7

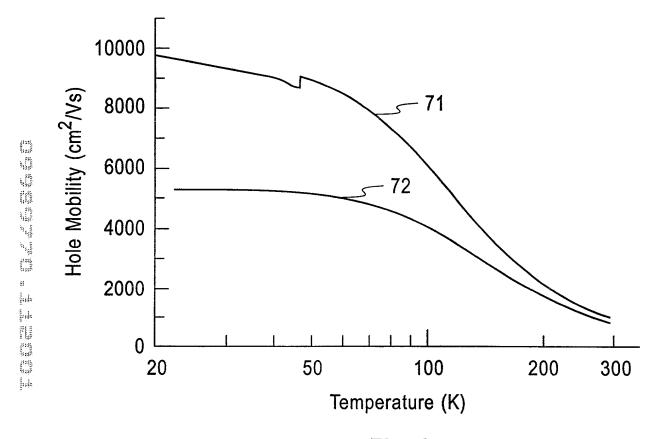


Fig. 8

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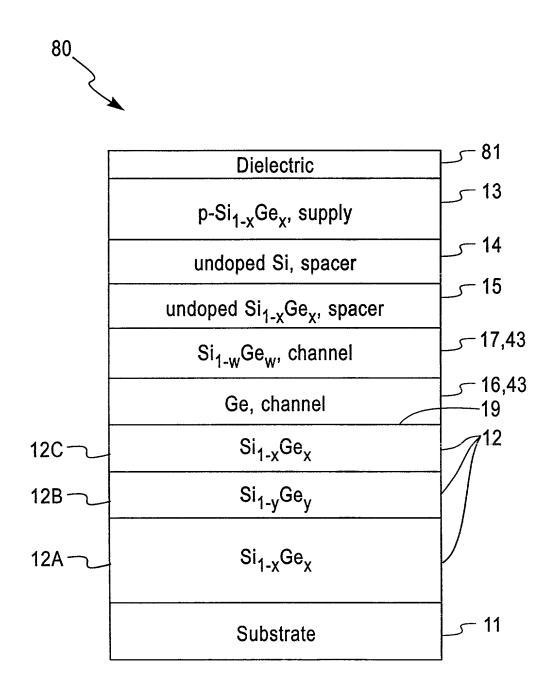
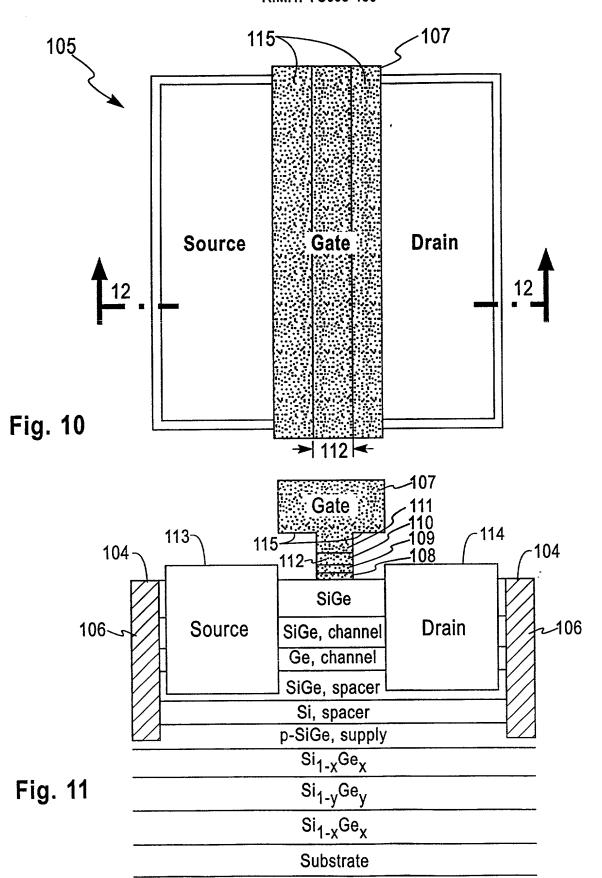


Fig. 9

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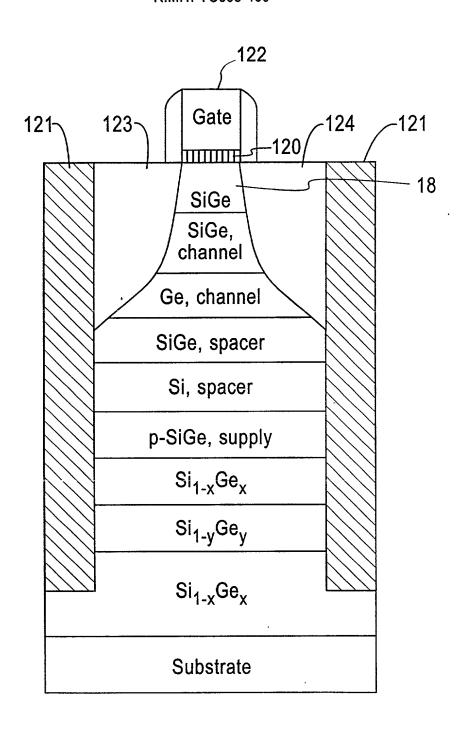


Fig. 12

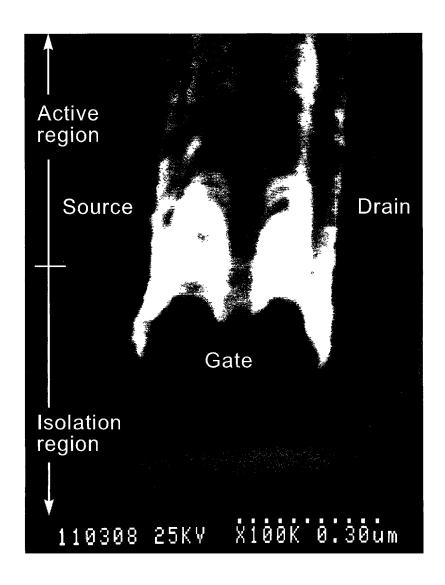


Fig. 13

p-type composite-channel MODFET,  $L_{\text{q}}$  = 0.09 $\mu$ m, W = 25 $\mu$ m

